ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Distributed Computing

Prof. R. Wattenhofer

Event-based data classification with Differentiable Logic Gate Networks

Machine learning models are often huge, which causes them to have high latency, low throughput, and high energy usage. In response to this, methods such as DiffLogic [1, 2, 3, 4], a logic-gate-based neural network architecture designed for FPGA acceleration (see in Figure 1), offer an efficient computational alternative.

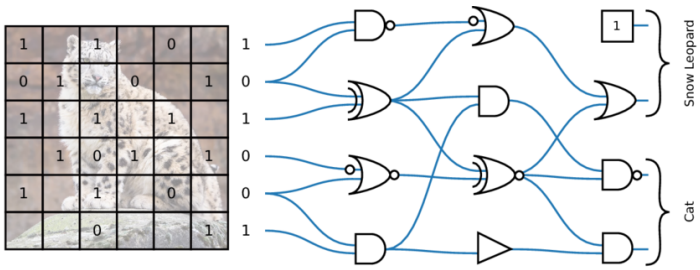

Figure 1: Overview of DiffLogic for image classification.

The high latency of machine learning models can be a significant issue in areas such as robotics that require very low-latency predictions. The latency requirements are so strict that classic cameras are often too slow in such domains. As such, one might opt for event-based cameras, which have very low latency.

This project will explore the application of difflogic models for classifying samples from existing event-based datasets.

The project will be done fully remote. We would have weekly meetings on Zoom to go over results, discuss open questions, and resolve any potential problems. You will have a lot of possibilities to shape the project in the directions you find the most interesting.

Requirements

Solid programming skills in Python and knowledge of machine learning evaluation are required. Experience exploring and visualizing large datasets, and experience with FPGAs are beneficial.

Contact

In a few short sentences, please describe your interest in this project and any relevant coding experience or background (e.g., projects or coursework).

- Andreas Plesner: aplesner@ethz.ch, ETZ G95
- Till Aczel: taczel@ethz.ch, ETZ G60.1

References

[1] Simon Bührer et al. *Recurrent Deep Differentiable Logic Gate Networks*. Aug. 2025. DOI: 10.48550/arXiv.2508.06097. arXiv: 2508.06097.

[2] Felix Petersen et al. "Convolutional differentiable logic gate networks". In: *Advances in Neural Information Processing Systems* 37 (2024), pp. 121185–121203.

[3] Felix Petersen et al. "Deep differentiable logic gate networks". In: *Advances in Neural Information Processing Systems* 35 (2022), pp. 2006–2018.

[4] Lukas Rüttgers et al. *Light Differentiable Logic Gate Networks*. Sept. 2025. DOI: 10.48550/arXiv.2510.03250. arXiv: 2510.03250.